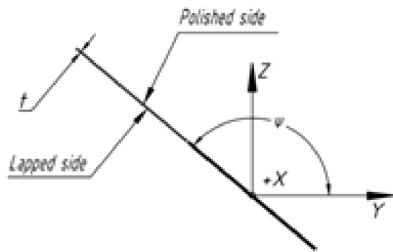
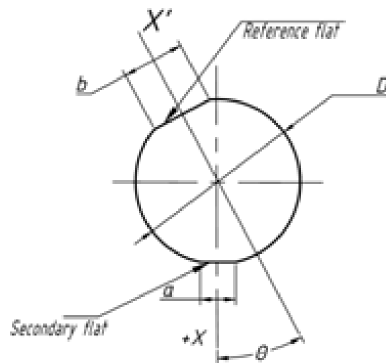
Wafer
LGS (0;138.5;26.7) 0.5xD76-LP





Wafer from synthetic Lanthanum Gallium silicate ($La_3Ga_5SiO_{14}$)		***Tolerance***
Cut, Ψ°	138.5°	± 10′
Cut, Θ°	26.7°	± 15′
Diameter D, mm	76.2	± 0.25
Thickness T, mm	0.50	± 0.03
Reference Flat F1, mm	22.0	± 3.0
Secondary Flat F2, mm	11.2	± 4.0
SURFACE		
Front Surface Finish	Polished, Ra ≤ 0.7 nm	
Back Surface Finish	Lapped, Ra ≤ 0.5 µm	
Flatness	≤10 µm	
Requirements to the surface of the wafer		
Working area of the wafer	3 mm smaller than the diameter of the wafer	
Scratches, cracks, contamination, others (dimples, pits, orange peel)	Not allowed on the working area by visual inspection	
Chips		
A) Inside the working area on both sides and on the reference flat B) Outside the working area of the wafer	A) not allowed B) Chips with the length no more than 1,0 mm and the width no more than 0,5mm are allowed.	
Bevel	Rounded edge	